DATA SHEET

SAA2520
Stereo filter and codec for MPEG layer 1 audio applications

Preliminary specification
File under Integrated Circuits, IC01

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Philips
Semiconductors

PHILIPS

Stereo filter and codec for MPEG layer 1 audio applications

SAA2520

FEATURES

- Stereo filtering and codec functions in a single chip
- MPEG coded interface
- Filtered data interface
- Baseband audio data interface
- LT interface to microcontroller
- Clock generator
- Low operating voltage capability.

GENERAL DESCRIPTION

The SAA2520 performs the sub-band filtering and audio frame codec functions to provide efficient audio compression/decompression for MPEG (11172-3) Layer1 applications. It is capable of functioning as a stand-alone decoder but requires the addition of an adaptive masking threshold processor (SAA2521) in order to function as a highly efficient encoder.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2520GP[1]	44	QFP	plastic	SOT205AG

Note

1. SOT205-1; 1996 August 26.

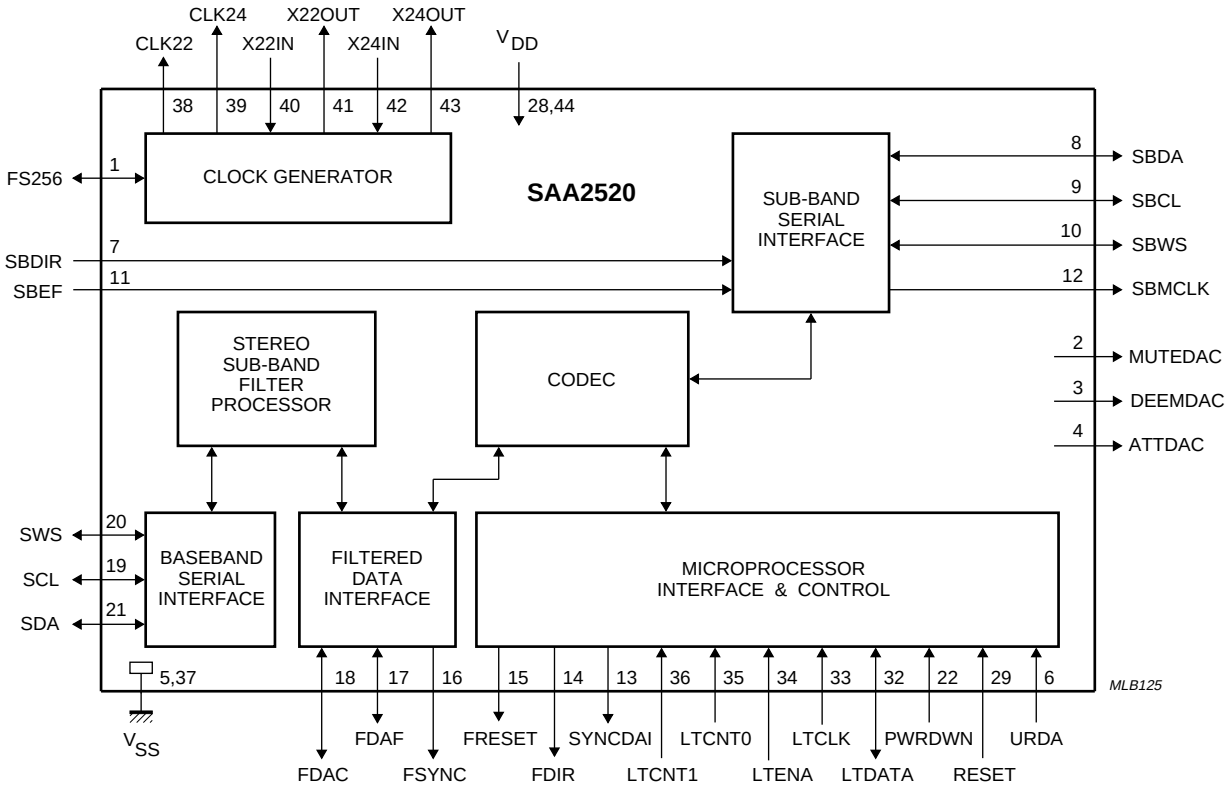


Fig.1 Block diagram.

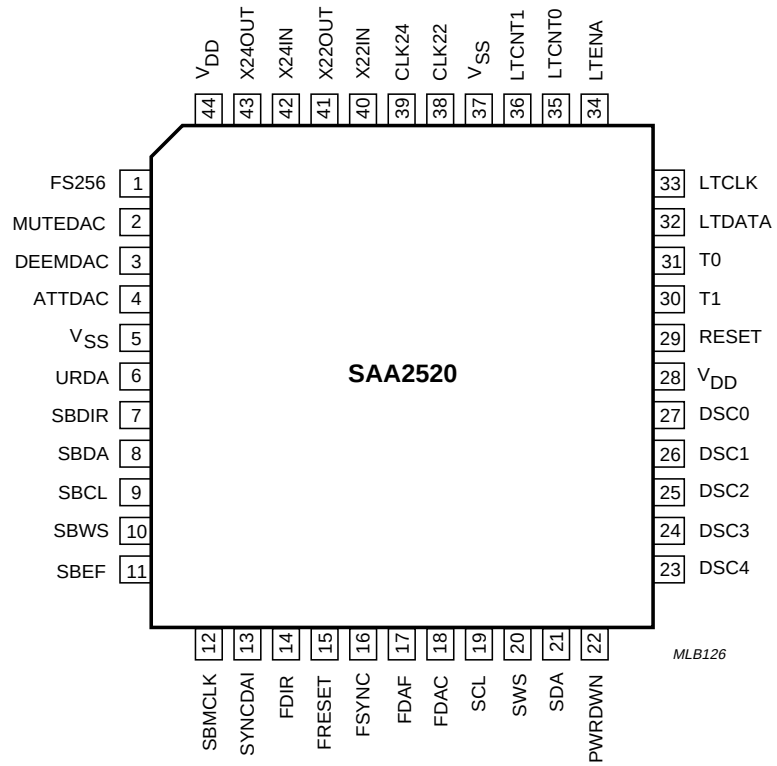


Fig.2 Pin configuration.

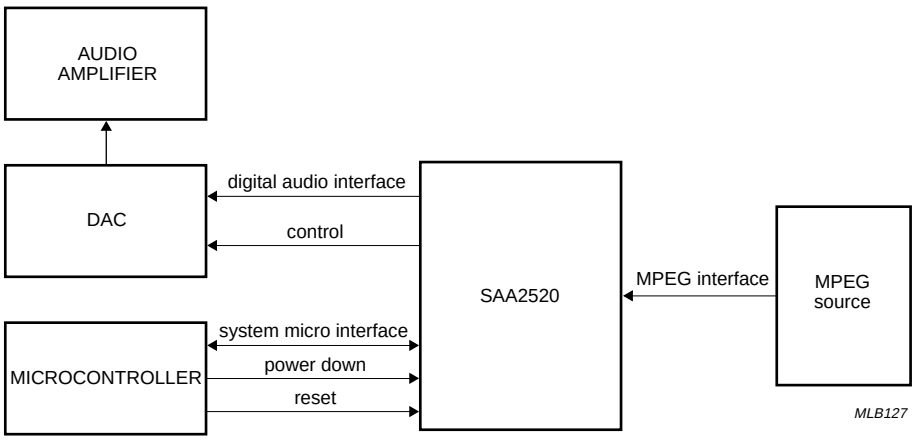


Fig.3 MPEG decoder system data flow diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
FS256	1	(Filtered)-I²S clock; 256 × sample frequency. 12 mA 3-state output + CMOS input with pull-down	I/O
MUTEDAC	2	DAC control/output expander	O
DEEMDAC	3	DAC control/output expander	O
ATTDAC	4	DAC control/output expander	O
V_{SS}	5	supply ground (0 V)	
URDA	6	unreliable drive processing data; CMOS level	I
SBDIR	7	sub-band I²S direction: (SWBS, SBCL, SBDA); CMOS level	I
SBDA	8	sub-band I²S data; 4 mA, 3-state output + CMOS input with pull-down	I/O
SBCL	9	sub-band I²S bit clock; 4 mA, 3-state output + CMOS input with pull-down	I/O
SBWS	10	sub-band I²S word select; 4 mA, 3-state output + CMOS input with pull-down	I/O
SBEF	11	sub-band I²S byte error flag; CMOS level	I
SBMCLK	12	sub-band I²S clock, 6.144 MHz locked to FS256; 8 mA, 3-state output + CMOS input with pull-down	O
SYNCDAI	13	DAI synchronization pulse	O
FDIR	14	(Filtered)-I²S direction: (FDAC, FDAF, SDA);	O
FRESET	15	reset signal for SAA2521	O
FSYNC	16	Filtered-I²S sync signal for SAA2521	O
FDAF	17	Filtered-I²S sub-band filter data; 4 mA, 3-state output + CMOS input with pull-down	I/O
FDAC	18	Filtered-I²S sub-band codec data; 4 mA, 3-state output + CMOS input with pull-down	I/O
SCL	19	I²S bit clock; 4 mA, 3-state output + CMOS input with pull-down	I/O
SWS	20	I²S-word select; 4 mA, 3-state output + CMOS input with pull-down	I/O
SDA	21	I²S baseband data filter; 4 mA, 3-state output + CMOS input with pull-down	I/O
PWRDWN	22	power-down mode; CMOS level	I
DSC4	23	test pin	
DSC3	24	test pin	
DSC2	25	test pin	
DSC1	26	test pin	
DSC0	27	test pin	
V_{DD}	28	positive supply voltage (+5 V)	
RESET	29	system reset; CMOS level with pull-down and hysteresis	I
T1	30	test pin; do not connect	
T0	31	test pin; do not connect	
LTDATA	32	LT interface data; 4 mA, 3-state output + CMOS input with pull-down	I/O
LTCLK	33	LT interface bit clock; CMOS level	I

SYMBOL	PIN	DESCRIPTION	TYPE
LTENA	34	LT interface enable; CMOS level	I
LTCNT0	35	LT interface control; CMOS level	I
LTCNT1	36	LT interface control; CMOS level	I
V_{SS}	37	supply ground (0 V)	
CLK22	38	22.5792 MHz buffered output	O
CLK24	39	24.576 MHz buffered output	O
X22IN	40	22.5792 MHz crystal input	I
X22OUT	41	22.5792 MHz crystal output	O
X24IN	42	24.576 MHZ crystal input	I
X24OUT	43	24.576 MHz crystal output	O
V_{DD}	44	positive supply voltage (+5 V)	

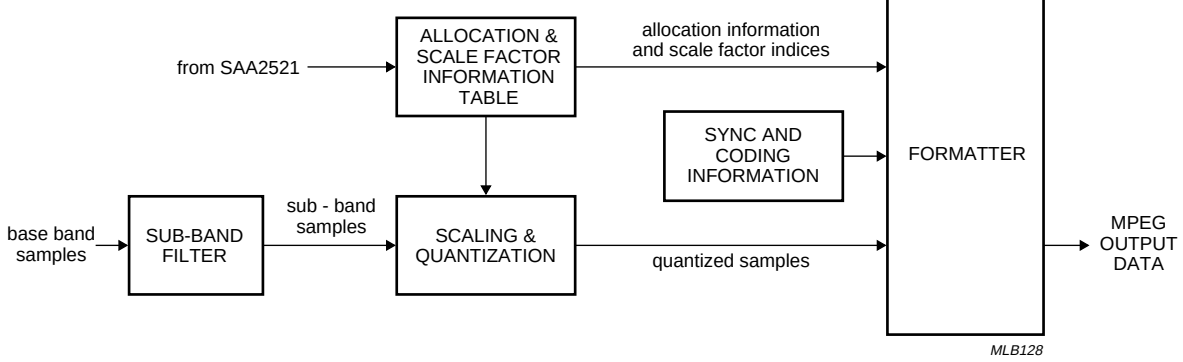


Fig.4 Encoding mode.

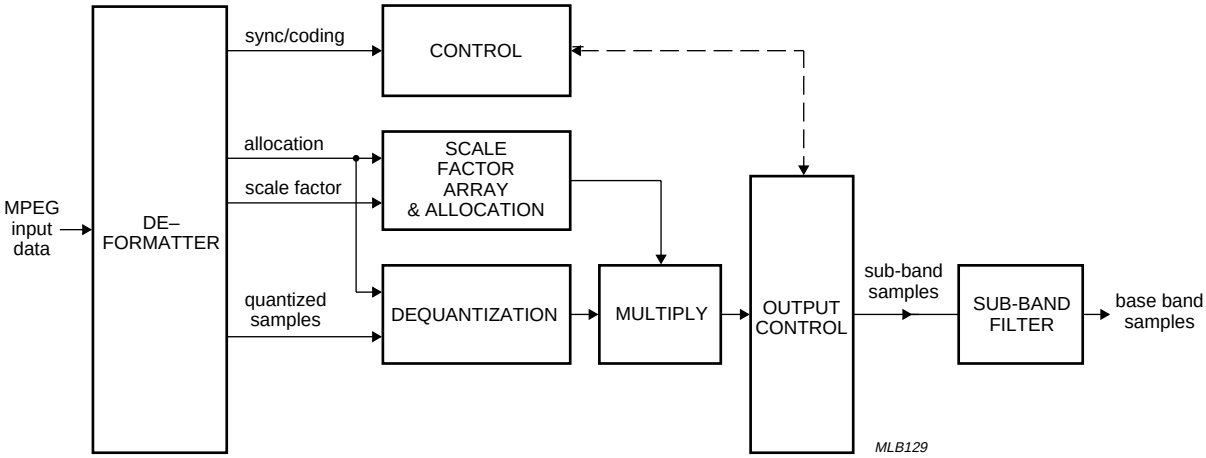


Fig.5 Decoding mode.

FUNCTIONAL DESCRIPTION

Coding System

MPEG coding achieves highly efficient digital encoding of audio signals by using an algorithm based on the characteristics of the human auditory system.

The broad-band audio signal is split into 32 sub-band signals during encoding. For each of the sub-band signals the masking threshold is calculated. The samples of the sub-bands are incorporated in the signal with an accuracy that is determined by the signal to masking threshold ratio for that sub-band.

During decoding, the sub-band signals are reconstructed and combined into a broadband audio signal. The integrated filter processor performs the splitting (encoding) and joining (decoding) including the corresponding formatting functions.

For encoding, a SAA2521 is necessary to calculate the masking threshold and required accuracy of the sub-band samples.

Encoding (See Fig.4)

An encoding algorithm table is used during the coding process but, due to the Adaptive Allocation functions of the SAA2521, this may change with every frame. The table is therefore calculated for each frame by the SAA2521 and then transferred to the SAA2520.

A frame contains 2×384 samples of Left and Right audio data. This results in 12 samples per sub-band (32 sub-bands). The samples of the greatest amplitude are used to determine the scale factor for a given sub-band. All samples are then scaled to represent a fraction of the greatest amplitude.

Once scaled, the samples are quantized to reduce the number of bits to correspond with the allocation table as calculated by the SAA2521. Synchronization and coding information data is then added to result in a fully encoded MPEG signal.

Decoding (See Fig.5)

All essential information (synchronization, system information, scale factors and encoded sub-band samples) are conveyed by incoming data. Decoding is repeated for every frame.

After sync and coding information, allocation data and the scale factors are used to correctly fill the scale factor array.

This is followed by a process of multiplication to provide de-quantization and de-scaling of the samples.
The decoded sub-band samples, which are represented in 24-bit two's complement notation, are processed by the sub-band filters and reconstituted into a single digital audio signal.

RESET

Reset must be active under the following conditions:

1. From system power-up until CLK24 has executed more than 24 clock cycles.
2. From the falling edge of PWRDWN for a period equivalent to 24 cycles of CLK24 + oscillator start-up time. This is typically >1 ms, however, this value is crystal dependent.

PWRDWN

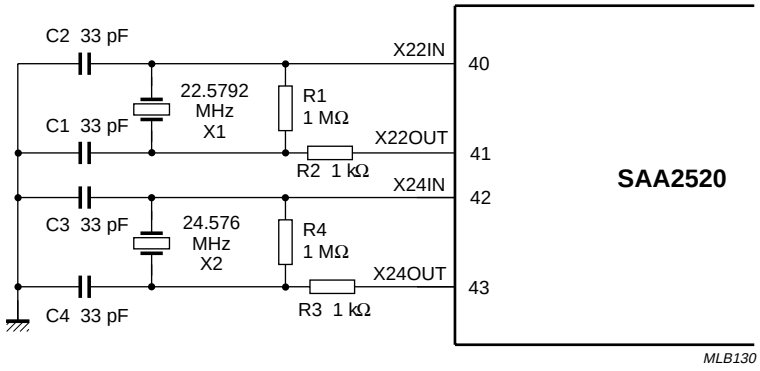
A HIGH input applied to this pin will halt all internally generated clock signals. As a result, chip activity will halt completely with outputs frozen in the state which was current at the time of PWRDWN activation.

The bi-directional outputs: LTDATA, FDAC, FDAF, SDA, SBWS, SBCL and SBDA will be 3-stated.

Crystal Oscillators

A 24.576 MHz crystal together with some external components form the 24.576 MHz oscillator (pins 42 and 43). Similarly a 22.5792 MHz oscillator (pins 40 and 41) is formed by similar peripheral components together with an appropriate crystal (see Fig.6).

The component values shown apply only to crystals from the Philips 4322 156 series which exhibit an equivalent series resistance of $\leq 40\ \Omega$.



Component values apply only to crystals from the Philips 4322 156 series.

Fig.6 Crystal oscillator components.

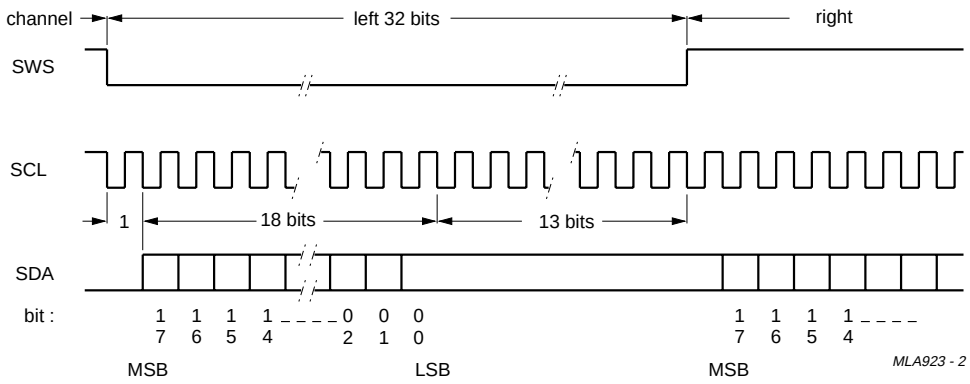


Fig.7 Transfer of SDA data (Standard I^2S default format).

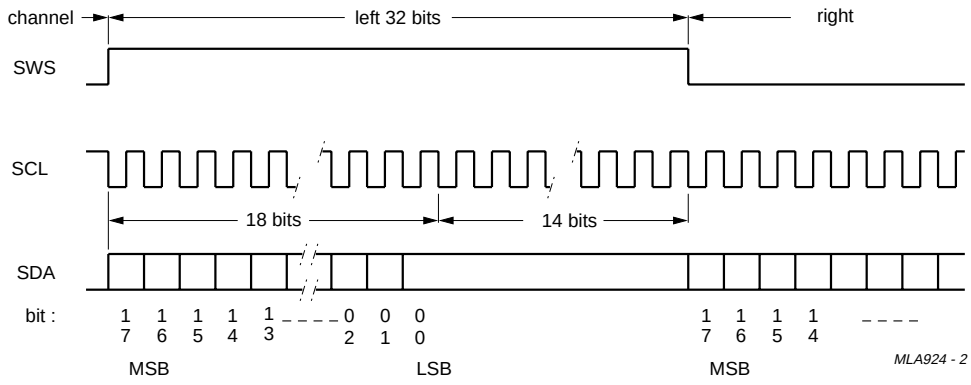


Fig.8 Transfer of SDA data (alternative format).

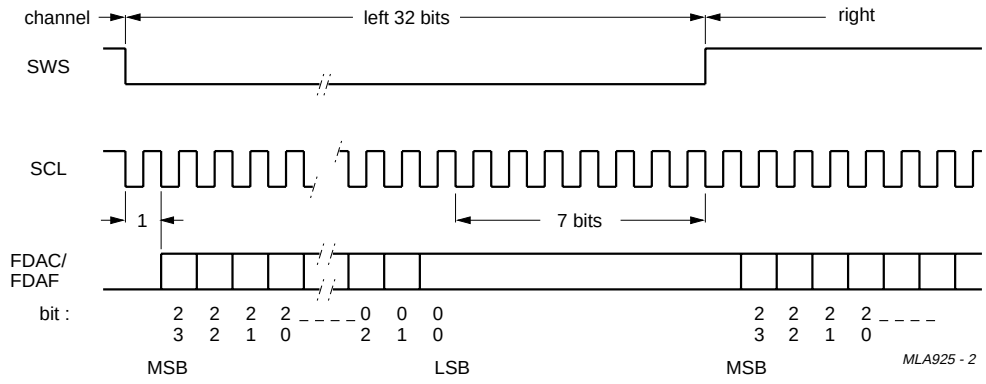


Fig.9 Transfer of FDAF and FDAC (filtered) data.

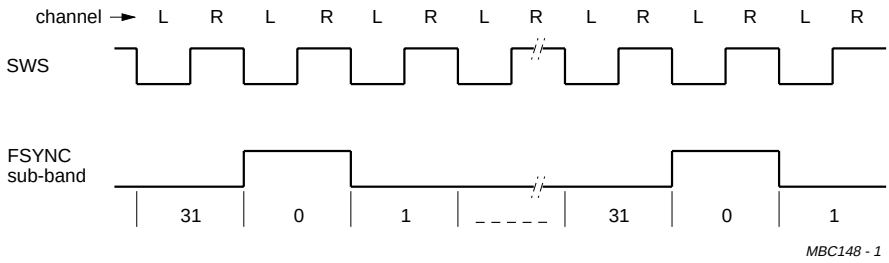


Fig.10 SWS related to phase of FSYNC.

Baseband Interface Signals

The interface between the SAA2520 and the baseband input/output circuitry consists of the following signals:

SWS	bi-directional	word (channel) select	FS
SCL	bi-directional	bit clock	64FS
SDA	bi-directional	baseband data	
FDIR	output	decoding mode (direction control)	

The SWS signal indicates the channel of the sample signal (either LEFT or RIGHT) and is equal to the sampling frequency FS.

Operating at a frequency of 64 times that is used for sampling, the bit clock dictates that each SWS period contains 64 SDA data bits. Of these, a maximum of 36 are used to transfer data (samples may have a length up to 18-bits). Samples are transferred most significant bit first. Both SWS and SDA change state at the negative edge of SCL.

This baseband data is transferred between the SAA2520 and the input/output using either Standard I^2S (default) or the alternative format shown in Fig.8.

Interface between SAA2520 and SAA2521 consists of the following signals:

FILTERED-I^2S INTERFACE

SWS	bi-directional	word select (common to I^2S)	FS
SCL	bi-directional	bit clock (common to I^2S)	64FS
FDAC	bi-directional	codec data	
FDAF	bi-directional	filter data	
FSYNC	output	synchronization	FS/32

Filtered data is transferred between SAA2520 filter/codec functions and the SAA2521 using the format shown in Fig.9.

The frequency of the SWS signal is equal to the sample frequency FS and the bit clock SCL is 64 times the sample frequency. Each period of SWS contains 64 data-bits, 48 of which are used to transfer data. The half period in which SWS is LOW is used to transfer the information of the LEFT channel while the following half period during which SWS is HIGH carries the data of the RIGHT channel. The 24-bit samples are transferred most significant bit first. This bit is transferred in the bit clock period with a 1-bit delay following the change in SWS. Both SWS and FDAF/FDAC change state at the negative edge of SCL.

The SAA2521 may be synchronized to the sub-band codec using the FSYNC signal, which defines the SWS period in which the samples of sub-band 0 (containing the lowest frequency components) are transferred (see Fig.10).

SAA2521 AND INPUT/OUTPUT MODE CONTROL

The operation of SAA2521 and the input/output circuitry is controlled by three signals shown in Table 1.

FRESET and SYNCDAI are given whenever:

- FS256, SCL and SWS outputs switch between high and low impedance
- FS256 frequency is changed (12.288/11.2896/8.192 MHz)
- FDIR is switching
- bit rate is changing
- system reset is active

MPEG CODED INTERFACE

The interface that carries the MPEG coded signal uses the following signals:

The MPEG I^2S interface

SBWS	bi-directional	word selection
SBCL	bi-directional	bit clock
SBDA	bi-directional	sub-band coded data
SBEF	input	error signal

Operation is further controlled by:

SBDIR	input	direction of data flow
URDA	input	unreliable encoded data signal

The SBMCLK signal is the main frequency from which other clock signals are derived. In encode mode this division is performed internally. In decode mode the external source should provide SBWS and SBCL. The frequency of the signal is equal to 1/32nd of the bit rate. The frequency of the bit clock SBCL is twice that of the bit rate. Some examples of the frequencies are given in Table 2.

Table 1 SAA2521 input/output control.

FRESET	output	request a general reset of SAA2521
FDIR	output	'1' for decoding and '0' for encoding mode (common to I^2S)
SYNCDAI	output	pulse for synchronization of digital input/output (TDA1315)

Table 2 Frequency examples.

BIT RATE (k BITS/s)	SBWS FREQUENCY (kHz)	SBCL FREQUENCY (kHz)
384	12	768
256	8	512
192	6	384
128	4	256

ENCODE MODE

The following modes are supported:

Stereo or 2-channel mono with allowable bit rates of 384, 256, 192 and 128 kbits/s; audio sampling frequencies of 48, 44.1 and 32 kHz.

DECODE MODE

The following modes are supported:

Stereo and joint stereo, 2-channel mono and 1-channel mono with allowable bit rates in the range 448 to 32 k bits/s; audio sampling frequencies of 48, 44.1 and 32 kHz.

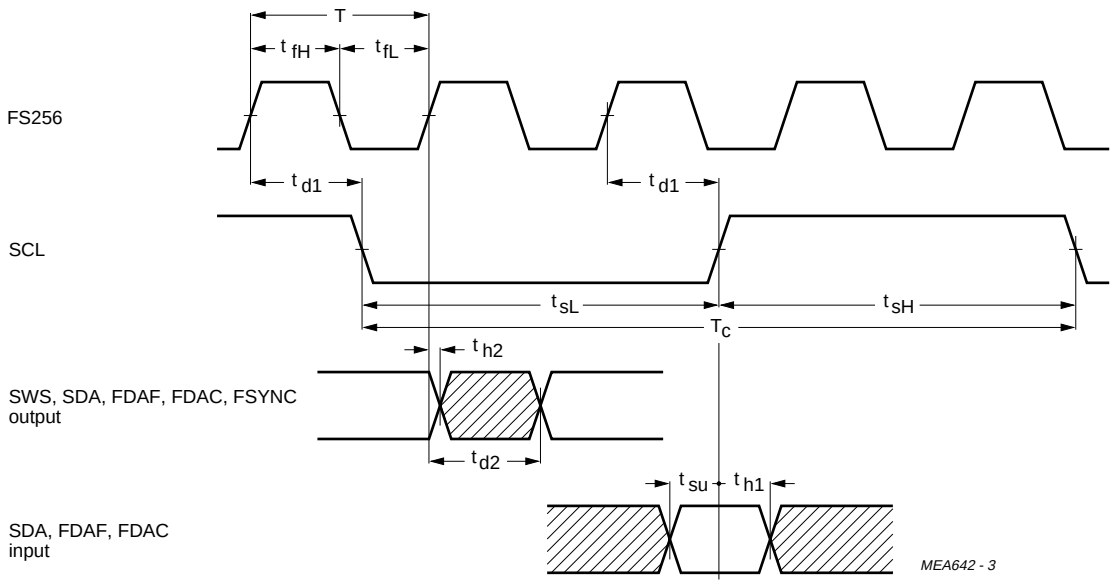


Fig.11 Filtered I²S interface timing (master mode - FS256, SCL and SWS are input).

Notes to Fig.11

T	FS256 cycle time (f_s = 48 kHz)	81.4 ns nominal
	FS256 cycle time (f_s = 44.1 kHz)	88.6 ns nominal
	FS256 cycle time (f_s = 32 kHz)	122.1 ns nominal
T_c	SCL cycle time	4T ns nominal
t_{fH}	FS256 HIGH time (f_s = 48 kHz)	≥ 35 ns
	FS256 HIGH time (f_s = 44.1 kHz)	≥ 38 ns
	FS256 HIGH time (f_s = 32 kHz)	≥ 35 ns
t_{fL}	FS256 LOW time (f_s = 48 kHz)	≥ 35 ns
	FS256 LOW time (f_s = 44.1 kHz)	≥ 38 ns
	FS256 LOW time (f_s = 32 kHz)	≥ 75 ns
t_{SH}	SCL HIGH time	≥ 2T - 20 ns
t_{SL}	SCL LOW time	≥ 2T - 20 ns
t_S	SDA, FDAF, FDAC input set-up before FS256 HIGH	≥ 20 ns
t_{H1}	SDA, FDAF, FDAC input hold after FS256 HIGH	≥ 30 ns
t_{H2}	SDA, FDAF, FDAC output hold after FS256 HIGH	≤ 0 ns
$t_{D1, 2}$	FS256 HIGH to SCL, SWS, SDA, FDAF, FDAC output valid	≤ 50 ns

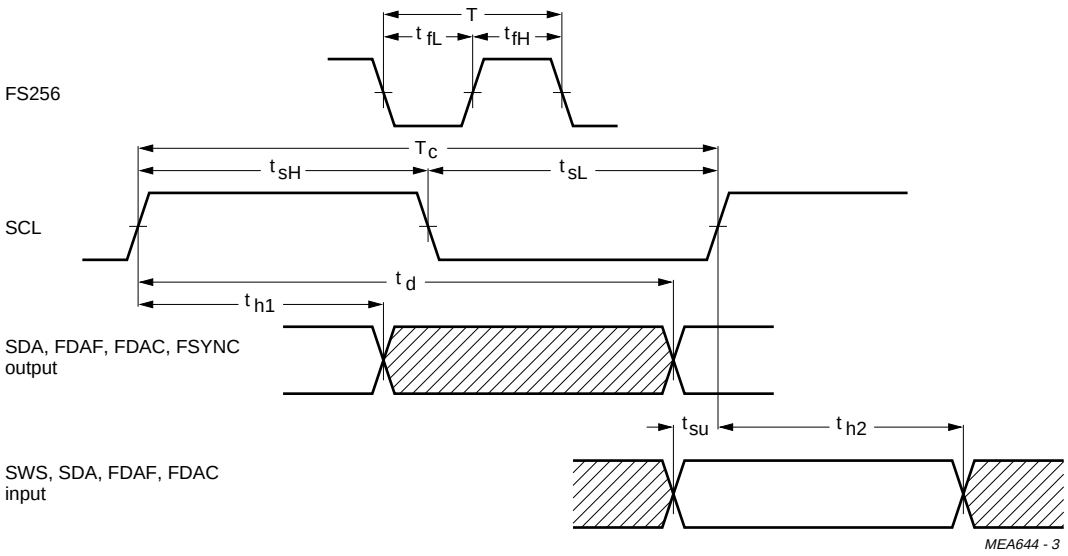


Fig.12 Filtered I^2S interface timing (slave mode - FS256, SCL and SWS are input).

Notes to Fig.12

t_{fH}	FS256 HIGH time	≥ 35 ns
t_{fL}	FS256 LOW time	≥ 35 ns
t_{sH}	SCL HIGH time	≥ T + 35 ns
t_{sL}	SCL LOW time	≥ T + 35 ns
t_{H1}	SDA, FDAF, FDAC output hold after SCL HIGH	≥ 2T - 15 ns
t_D	SCL HIGH to SDA, FDAF FDAC output valid	≤ 3T + 60 ns
t_s	SDA, FDAF, FDAC input valid after SCL HIGH	≥ 20 ns
t_{H2}	SDA, FDAF, FDAC input hold after SCL HIGH	≥ T + 20 ns

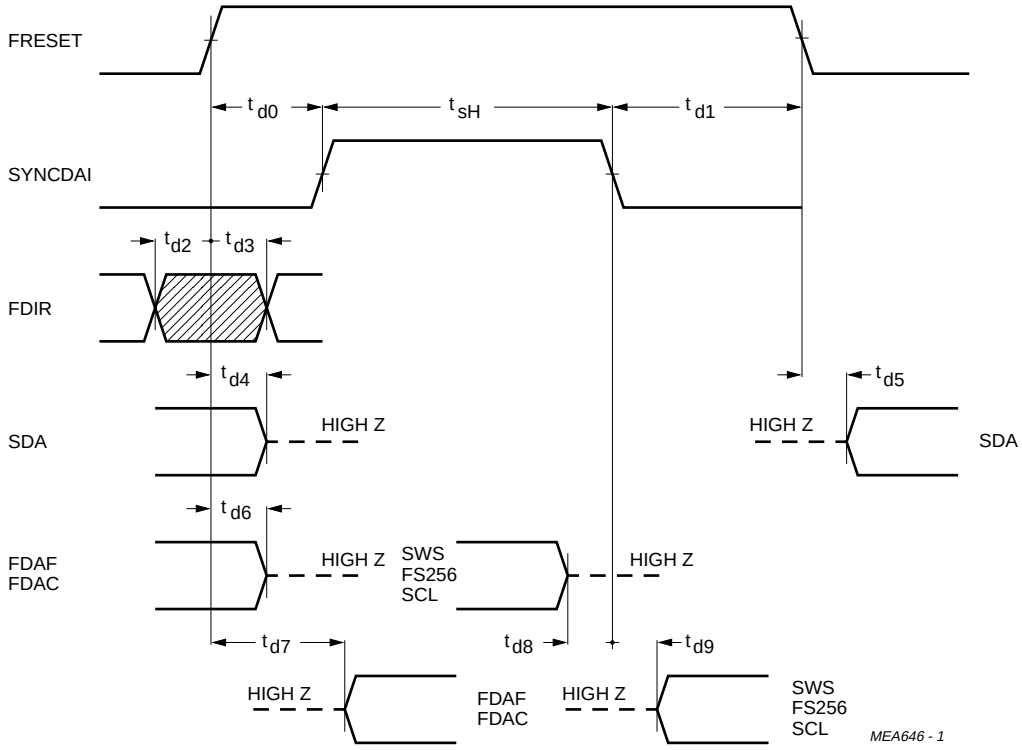


Fig.13 Mode switch timing.

Notes to Fig.13

t_{DO}	FRESET HIGH to SYNCDAI HIGH	≥ 300 ns
t_{SH}	SYNCDAI HIGH time	≥ 1280 ns
t_{D1}	SYNCDAI LOW to FRESET LOW	≥ 790 ns
t_{D2}	FDIR hold to FRESET HIGH	≤ 20 ns
t_{D3}	FRESET HIGH to FDIR valid	≤ 20 ns
t_{D4}	SDA change to high impedance after FRESET HIGH	≥ 0 ns ≤ 170 ns
t_{D5}	SDA remains high impedance after FRESET LOW	≥ 0 ns ≤ 170 ns
t_{D6}	FDAF, FDAC change to high impedance after FRESET HIGH	≤ 20 ns
t_{D7}	FDAF, FDAC remain high impedance	

Notes to Fig.13

	after FRESET HIGH	≥ 460 ns
t_{D8}	FS256, SWS, SCL change to high impedance before SYNCDAI HIGH	≥ 140 ns
t_{D9}	FS256, SWS, SCL remain HIGH impedance after SYNCDAI HIGH	≥ 140 ns

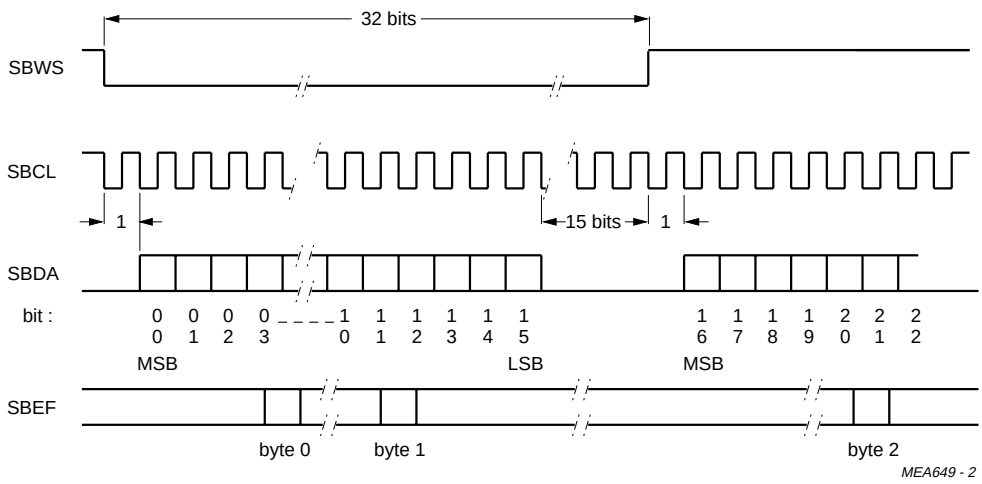


Fig.14 Transferring MPEG data to and from the SAA2520.

MPEG Coded Interface (Sub-band I^2S)

The MPEG coded data is transferred to and from the SAA2520 using the format shown in Fig.14.

Each period of SBWS contains 64 data bits, 32 of which are used to convey data. The half-period during which SBWS is logic 0 is used to transfer the first 16-bits (0 to 15) of a sub-band slot. The remaining half-period during which SBWS is logic 1 carries the remaining 16-bits (16 to 31). Thus one period of SBWS corresponds with one slot of the sub-band signal.

Bits 0 and 16 are transferred in the bit clock period, one bit-time after the change in SBWS. Both SBWS and SBDA change state during the negative edge of SBCL.

In decode mode a byte error flag SBEF is also transferred. This occurs approximately in the middle of the corresponding byte (byte 0 = bits 0 to 7, byte 1 = bits 8 to 15 etc).

Encoding mode

SBCL, SBWS and SBDA are generated by the SAA2520. However, if the SBDIR signal is logic 1, the output buffers are not enabled and these signals do not appear on the pins. This mode is available to permit a change of operating mode whilst the bus signals are driven from an external source.

Decoding mode

SBCL, SBWS and SBDA are generated by an external source.

Table 3 contains a summary of the source signals in the various modes.

Table 3 Modes and source signals.

			source of:					
Mode	**FDIR**	**SBDIR**	**SBWS**	**SBCL**	**SBDA**	**SBEF**	**SBMCLK**	
Encode	0	0	INT	INT	INT	----	INT	note 1
Encode	0	1	EXT	EXT	EXT	----	INT	note 2
Decode	1	0	INT	INT	INT	EXT	INT	note 3
Decode	1	1	EXT	EXT	EXT	EXT	INT	

Notes

1. During encoding the SBEF signal is ‘don’t care’.
2. Incoming data is not decoded. The SAA2520 operates in the encoding mode and the data does not enter the interface.
3. Operation is undefined. The SAA2520 is in decoding mode whilst the SBWS, SBCL and SBDA output drivers are enabled.

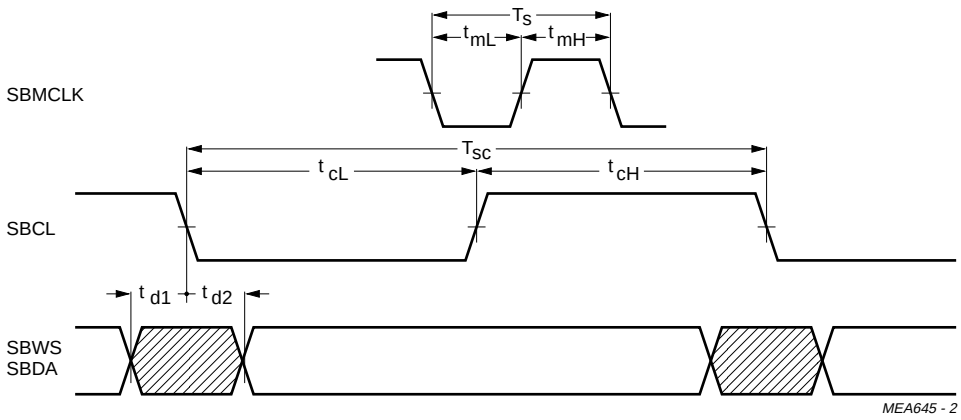


Fig.15 Sub-band I^2S interface timing (master mode - SBCL, SBWS and SBDA are output).

Notes to Fig.15

T	SBMCLK cycle time	120 to 205 ns (163 ns nominal)
t_{mH}	SBMCLK HIGH time	≥ 35 ns
t_{mL}	SBMCLK LOW time	≥ 75 ns
T_c	SBCL cycle time (384 kB/s)	8T ns nominal
	SBCL cycle time (256 kB/s)	12T ns nominal
	SBCL cycle time (192 kB/s)	16T ns nominal
	SBCL cycle time (128 kB/s)	24T ns nominal
t_{CH}	SBCL HIGH time (384 kB/s)	≥ 4T - 20 ns
	SBCL HIGH time (256 kB/s)	≥ 6T - 20 ns
	SBCL HIGH time (192 kB/s)	≥ 8T - 20 ns
	SBCL HIGH time (128 kB/s)	≥ 12T - 20 ns
t_{CL}	SBCL LOW time (384 kB/s)	≥ 4T - 20 ns
	SBCL LOW time (256 k/Bs)	≥ 6T - 20 ns
	SBCL LOW time (192 kB/s)	≥ 8T - 20 ns
	SBCL LOW time (128 kB/s)	≥ 12T - 20 ns
t_{D1}	SBWS, SBDA hold to SBCL LOW	≤ 20 ns
t_{D2}	SBCL LOW to SBWS, SBDA valid	≤ 20 ns

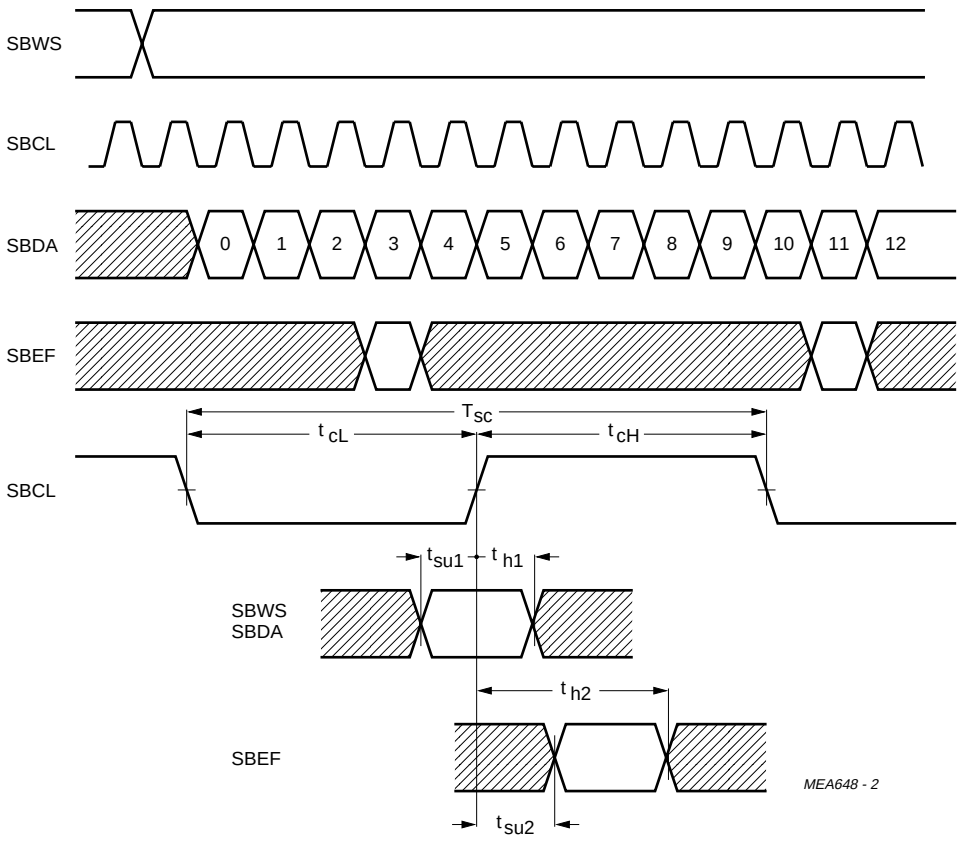


Fig.16 Sub-band I^2S interface timing (slave mode - SBCL, SBWS and SBDA are input).

Notes to Fig.16

T_C	SBCL cycle time (see note 1)	6.86T to 96T ns (8T ns nominal)
t_{CH}	SBCL HIGH time	≥ T + 30 ns
t_{CL}	SBCL LOW time	≥ T + 30 ns
t_{S1}	SBWS, SBDA input set-up before SBCL HIGH	≥ T + 30 ns
t_{H1}	SBWS, SBDA input hold after SBCL HIGH	≥ 30 ns
t_{S2}	SBCL HIGH to SBEF valid	≤ T - 30 ns
t_{H2}	SBEF hold after SBCL HIGH	≥ 2T- 30 ns

Note 1:
Minimum at bit rate = 448 kB/s
Nominal at bit rate = 384 kB/s
Maximum at bit rate = 32 kB/s

Fig.17 Sub-band I^2S mode switch timing.

Notes to Fig.17

t_{D1}	SBDIR HIGH to SBCL, SBWS, SBDA high impedance	≤ 50 ns
t_{D2}	SBCL, SBWS, SBDA after SBDIR LOW high impedance	≥ 240 ns

Microcontroller interface

The SAA2520 has an interface connection to the serial interface of a microcontroller. The following signals are used:

LTCLK	input	bit clock
LTDATA	bi-directional	serial data
LTCNT0	input	control line 0
LTCNT1	input	control line 1
LTENA	input	enable

The SAA2520 microcontroller interface is enabled only if LTENA (pin 34) is logic 1. Information to or from the SAA2520 is conveyed in serial 8 or 16-bit units, whilst the type of information is controlled by LTCNT0 (pin 35) and LTCNT1 (pin 36).

A transfer commences when the microcontroller sets the control lines to the correct combination for the required action. LTENA is set to logic 1. The SAA2520 determines its required action and prepares to transfer data. When the microcontroller supplies the LTCLK, data is transferred to or from the SAA2520 in units of 8-bits. 16-bit transfers are conveyed as two 8-bit units during which LTENA remains high.

During the transfer of 8-bit units, the least significant bit is first to be transferred. When 16-bit units are transferred the most significant byte is sent first.

EXTENDED SETTINGS (LTCNT1 = 0, LTCNT0 = 0)

Four information bits together with four address bits are transferred in this mode. The order in which the bits appear on the interface is:

D0..D1..D2..D3..A0..A1..A2..A3

Table 4 Extended Settings.

BIT A3	BIT A2	BIT A1	BIT A0	DESCRIPTION
0	0	0	0	CODEC external settings (see Table 5)
0	0	0	1	FILTER settings (see note 1)
0	0	1	0	not used
..	..	..	..	..
1	1	1	1	not used

Table 5 Extended Settings.

BIT	DESIGNATION	DEFAULT	FUNCTION
D0	MUTEDAC	1	connected to DAC mute input
D1	ATTDAC	0	connected to DAC attenuation input
D2	DEEMDAC	0	emphasis control for DAC circuit
D3	HOLDCLKOK	0	selects CLKOK hold mode

Note

If not used for DAC control, the MUTEDAC, ATTDAC and DEEMDAC can be used as general purpose output expanders.

Bits D0 to D3 are copied directly to the corresponding output pins/mode flip-flop.

For HOLDCLKOK = logic 1. When CLKOK drops it will remain LOW until set by an encode/decode mode, sample frequency, external 256FS or bit rate index change.

Note 1.

When D0 = logic 1 (default) I^2S mode is selected. For D0 = logic 0 the alternative mode is selected. The setting of D0 remains dormant until activated by the occurrence of FRESET.

ALLOCATION/SCALE FACTOR INFORMATION (LTCNT1 = LOGIC 0, LTCNT0 = LOGIC 1)

For encoding, the allocation and scale factor arrays can be filled using this mode. To completely fill the allocation array 16 complete transfers of 16-bits are required. After the first transfer of allocation information a check must be made to determine when the SAA2520 is ready to receive the remaining information. This will ensure synchronization with the internal program of the SAA2520. Transfer of the allocation information is completed by sending the internal settings.

This is then followed by the scale factor information.

In the event that only internal settings information is sent, then a default allocation of logic 0 will be assigned to all sub-bands. If in addition no internal settings are sent then the previous settings remain valid.

The allocation information is transferred in 4-bit units. Each of these units contains the number of bits allocated to the sub-band, MINUS 1, except in the case of a logic 0 value, which indicates that no bits are allocated to that sub-band.

Scale factor information is transferred in units of 8-bits, containing the 6-bit scale factor which is extended to 8-bits by adding two logic 0's at the most significant end.

In the case of stereo encoding the channels are indicated by L (left) and R (right). This changes to I and II in the case of 2 channel mono encoding.

Table 6 Allocation information format.

msb						lsb	channel	sub-band
		bits						
B15	-	B14	-	B13	-	B12	L or I	0 .. 30 (even)
B11	-	B10	-	B9	-	B8	R or II	0 .. 30 (even)
B7	-	B6	-	B5	-	B4	L or I	1 .. 31 (odd)
B3	-	B2	-	B1	-	B0	R or II	1 .. 31 (odd)

Table 7 Scalefactor information format.

msb	bits	lsb	channel	sub-band
B15	.....	B8	L or I	0 .. 31
B7	.....	B0	R or II	0 .. 31

INTERNAL SETTINGS (LTCNT1 = LOGIC 1, LTNCT 0 = LOGIC 0)

The operation of the codec is controlled by the bits transferred in this mode.

Table 8 Internal Settings (LTCNT1 = logic 1, LTNCT 0 = logic 0).

msb		lsb	name	function	valid in
S15	...	S12	bit rate index	bit rate indication	encode
S11	...	S10	sample frequency	44.1, 48 or 32 kHz indication	encode
S9			decode	1 = decode; 0 = encode	encode/decode
S8			EXT 256FS	1 = external; 0 = internal 256FS	encode/decode
S7			2-channel mono	1 = 2-CH mono; 0 = stereo	encode
S6			MUTE	1 = mute; 0 = no mute	encode/decode
S5				not used	
S4			CH1	1 = CH1; 0 = CH2	decode
S3	...	S2	Tr0 to Tr1	transparent bits	encode
S1	...	S0	EMPHASIS	emphasis indication	encode

Table 9 Internal Settings (LTCNT1 = logic 1, LTCNT0 = logic 0).

msb			lsb	bit rate	
1	1	0	0	384 kbits/s	default value
1	0	0	0	256 kbits/s	
0	1	1	0	192 kbits/s	
0	1	0	0	128 kbits/s	

The bit rate index indicates the bit rate of the encoded signal and is only effective in the encode mode.

The decode bit determines the operation mode of the SAA2520. The default value is logic 1 (decoding mode).

EXT 256FS in the encoding mode determines whether or not the SAA2520 is master or slave of the Filtered-I^{2}S interface (default is logic 0, master mode).

2CH MONO is used in the encoding mode to determine whether the sub-band signal is generated as a stereo or 2-channel mono signal. Default value is logic 0.

MUTE is used in both the encoding and decoding modes to mute the information to or from the Filtered-I^{2}S interface (the default value is logic 0).

CH1 is utilized in the decoding mode to select one of the 2-channel mono signals to be decoded (default is I - channel 1). A value of 0 results in channel 2 being decoded).

The transparent bits are copied in the sub-band signal, default is 00.

The information from S15 to S10, S7 and S3 to S0 will be copied into the sub-band signal.

Table 10 Sample frequency indication.

msb	lsb	sample frequency	
0	0	44.1 kHz	default value
0	1	48 kHz	
1	0	32 kHz	
1	1	not used	

Table 11 EMPHASIS indication.

msb	lsb	emphasis	
0	0	no emphasis	default value
0	1	50/15 µs	
1	0	reserved	
1	1	CCITT J.17	

Before sending internal settings the microcontroller should check whether or not the SAA2520 is ready-to-receive. However, this does not apply for the transfer of internal settings to end a transfer of allocation information.

STATUS (LTCNT = LOGIC 1, LTNCT0 = LOGIC 1)

Table 12 Status information 16-bit units.

msb		lsb	name	function	valid in
T15	...	T12	bit rate index	bit rate indication	encode/decode
T11	...	T10	sample frequency	44.1, 48 or 32 kHz indication	encode/decode
T9			ready-to-receive	1 = ready; 0 = not ready	encode/decode
T8			not used		
T7		T6	MODE	sub-band signal mode indication	encode/decode
T5			SYNC	synchronization indication	decode
T4			CLKOK	1 = o.k.; 0 = not o.k.	encode/decode
T3		T2	Tr0 to Tr1	transparent bits	encode/decode
T1	...	T0	EMPHASIS	emphasis indication	encode/decode

The bit rate index indicates the bit rate of the sub-band signal in units of 32 kbits/s. bit rate index 0000 indicates the ‘free format’ condition. bit rate 1111 is illegal and should not be found.

The coding of the sample frequency indication is equal to the one in the internal settings.

Table 13 MODE identification.

msb	lsb	mode	output
0	0	stereo	L and R
0	1	joint stereo	L and R
1	0	2 channel mono	I or II as selected
1	1	1 channel mono	mono; no selection

Ready-to-receive indicates whether the SAA2520 is ready to receive allocation, scale factor or internal setting transfers. This should be checked in order to synchronize the transfer of such information.

In 2 channel mono decode mode the selected samples are transferred to both output channels. The same occurs with all samples in 1-channel mono decode mode. In both of these instances the L and R filter output channels are identical.

In decode mode the SYNC bit is logic 0 when the SAA2520 is unable to decode the sub-band frames. This will occur in the following situations:

- with the loss of synchronisation
- when in correct allocation information is received for two or more subsequent frames (SBEF was HIGH).
- when the URDA input pin is HIGH

In these situations the SAA2520 data output will be muted. The SYNC bit will return to logic 1 as soon as the decoder is resynchronized to the incoming sub-band data.

CLKOK indicates whether the 256FS clock corresponds to specified sample frequency. The CLKOK bit is set to logic 1 after a change in sample frequency, operation mode or EXT256FS setting. It drops to logic 0 as soon as the 256FS clock deviates from the nominal frequency by more than approximately 0.2%. Return to logic 1 will only occur automatically when the extended setting CLKOK-hold-mode is logic 0.

The transparent bits are copied from the MPEG coded signal.

The EMPHASIS indication is as defined in the internal settings. It can be used to apply the correct de-emphasis.

Note: the two bytes of the status are 'sampled' at different moments so the information may not result from the same sub-band frame.

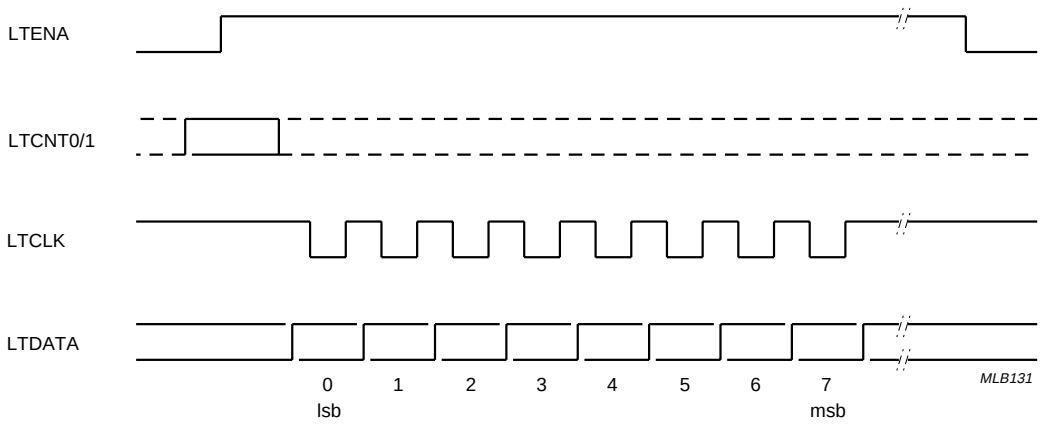


Fig.18 Transfer of data on SAA2520 microcontroller interface.

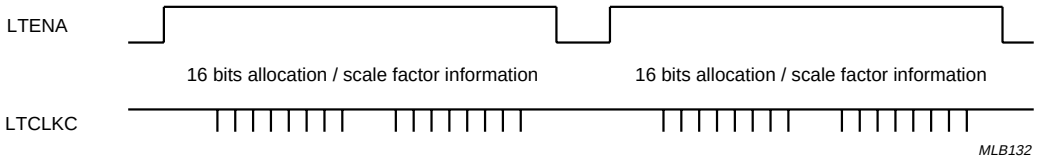


Fig.19 The LTENA line must return to logic 0 between information transfers.

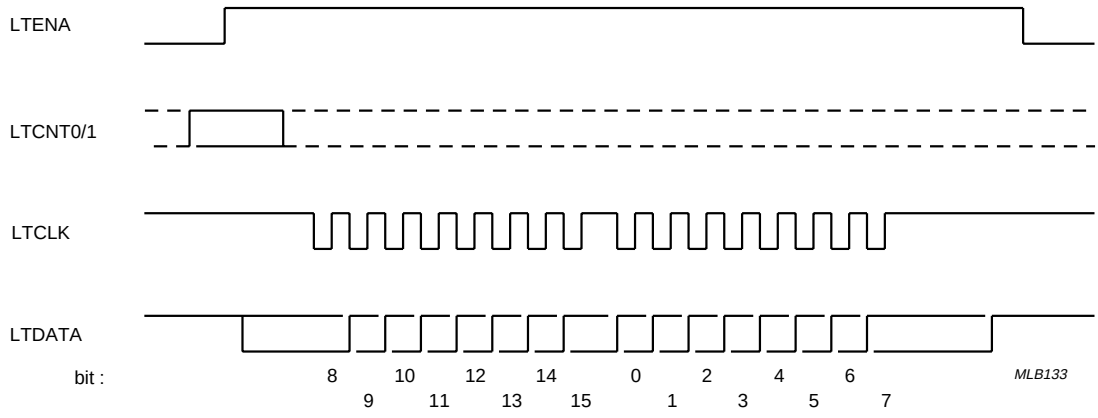
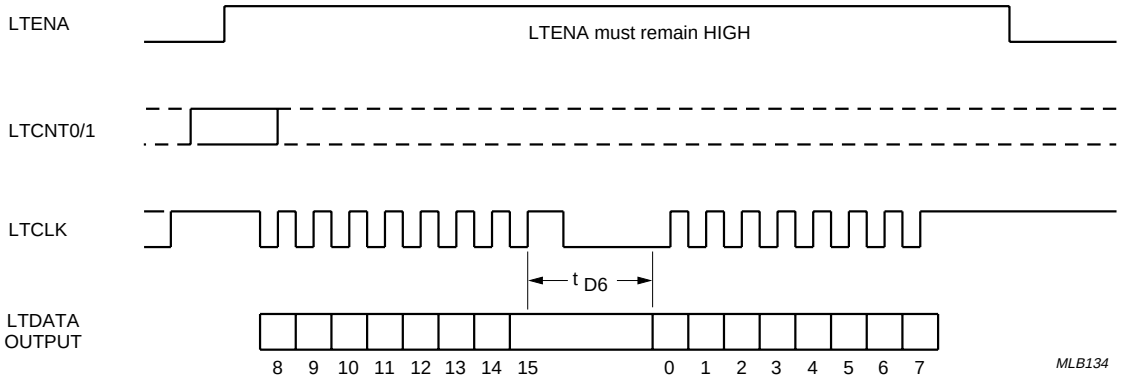


Fig.20 Order of settings and status bits on the SAA2520 microcontroller interface.



t_{D6} delay LTCLK HIGH to LTDATA valid output for bit 0 in 16-bit transfers

Fig.21 16-bit transfers.

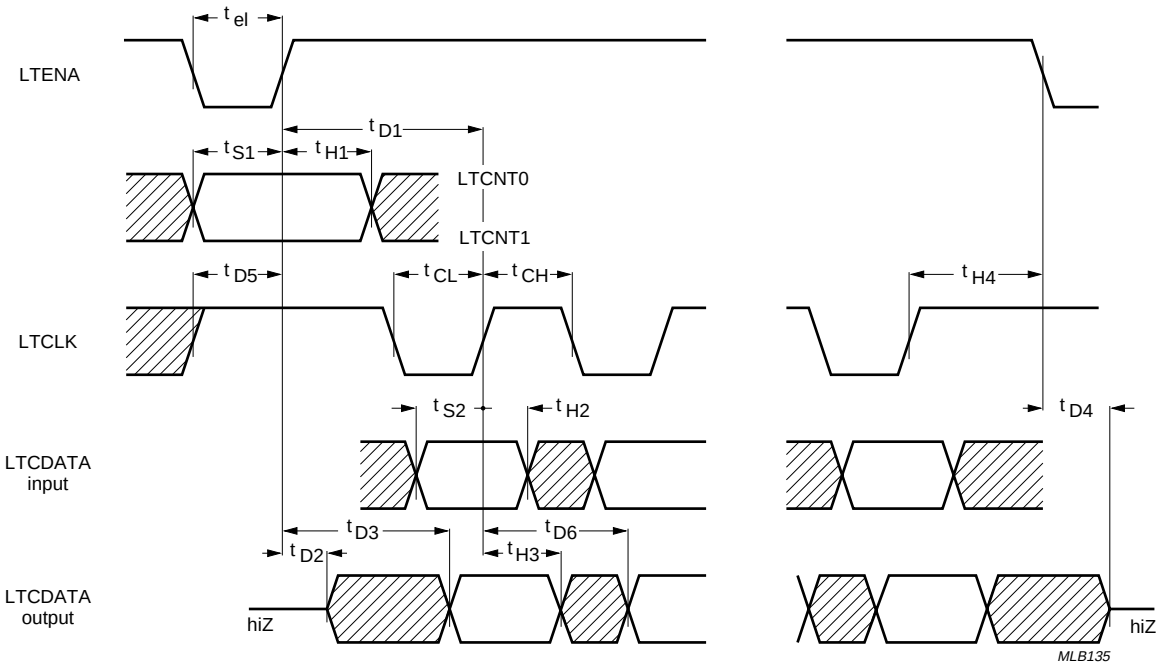


Fig.22 Microcontroller interface timing.

Notes to Fig.22

t_{eL}	LTENA LOW time	≥ 190 ns
t_{CH}	LTCLK HIGH time	≥ 190 ns
t_{CL}	LTCLK LOW time	≥ 190 ns
t_{D1}	LTENA HIGH to LTCLK HIGH	≥ 190 ns
t_{D2}	LTENA HIGH to LTDATA output low impedance	≥ 0 ns
t_{D3}	LTENA HIGH to LTDATA output valid	≤ 380 ns
t_{D4}	LTENA LOW to LTDATA high impedance	≤ 50 ns
t_{H4}	LTENA hold after LTCLK HIGH	≥ 355 ns
t_{D5}	LTCLK HIGH to LTENA HIGH	≥ 190 ns
t_{D6}	LTCLK HIGH to LTDATA output valid for bit 0 (see Fig.21)	≤ 355 ns
	for first bit in the second 8-bit unit	≤ 520 ns
t_{S1}	LTCNT0/1 set-up before LTENA HIGH	≥ 190 ns
t_{H1}	LTCNT0/1 hold after LTENA HIGH	≥ 190 ns
t_{S2}	LTDATA set-up before LTCLK HIGH	≥ 190 ns
t_{H2}	LTDATA input hold after LTCLK HIGH	≥ 30 ns
t_{H3}	LTDATA output hold after LTCLK HIGH	≥ 145 ns
t_{H4}	LTENA hold after LTCLK HIGH	≥ 355 ns

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	6.5	V
V_I	input voltage	note 1	–0.5	V_{DD} + 0.5	V
I_{SS}	supply current from V_{SS}		–	160	mA
I_{DD}	supply current in V_{DD}		–	160	mA
I_I	input current		–10	10	mA
I_O	output current		–20	20	mA
P_{tot}	total power dissipation		–	880	mW
T_{stg}	storage temperature range		–55	150	°C
T_{amb}	operating ambient temperature range		- 40	85	°C
V_{es1}	electrostatic handling	note 2	–1500	1500	V
V_{es2}	electrostatic handling	note 3	–70	70	V

Notes

1. Input voltage should not exceed 6.5 V unless otherwise specified
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor
3. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

DC CHARACTERISTICS

T_{amb} = –40 to 85 °C; V_{DD} = 3.8 to 5.5 V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.8	5.0	5.5	V
I_{DD}	operating current	V_{DD} = 5 V (note 1)	–	82	110	mA
I_{DD}	operating current	V_{DD} = 3.8 V (note 1)	–	58	80	mA
Inputs URDA, SBDIR, SBEF, LTCLK, LTCNT0, LTNCT1, X22IN, X24IN						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
$-I_I$	input current	V_i = 0 V; T_{amb} = 25 °C	–	–	10	µA
$+I_I$	input current	V_i = 5.5 V; T_{amb} = 25 °C	–	–	10	µA
Inputs PWRDWN, LTENA						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
$+I_I$	input current	V_i = V_{DD}; T_{amb} = 25 °C	40	–	250	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input RESET						
V_{tlh}	positive-going threshold		–	–	$0.8V_{DD}$	V
V_{thl}	negative-going threshold		$0.2V_{DD}$	–	–	V
V_{hys}	hystersis	$(V_{tlh} - V_{thl})$	–	1.5	–	V
$+I_I$	input current	$V_i = V_{DD}$; $T_{amb} = 25$ °C	40	–	250	µA
Outputs MUTEDAC, DEEMDAC, ATTDAC, SYNCDAI, FDIR, FRESET, FSYNC, CLK22						
V_{OH}	HIGH level output voltage	$+I_o = 2$ mA	$V_{DD}–0.5$	–	–	V
V_{OL}	LOW level output voltage	$–I_o = 2$ mA	–	–	0.4	V
Outputs CLK24						
V_{OH}	HIGH level output voltage	$+I_o = 8$ mA	$V_{DD}–0.5$	–	–	V
V_{OL}	LOW level output voltage	$–I_o = 8$ mA	–	–	0.4	V
Inputs/outputs SBDA, SBCL, SBWS, FDAF, FDAC, SCL, SWS, SDA, LTDATA						
V_{OH}	HIGH level output voltage	$+I_o = 2$ mA	$V_{DD}–0.5$	–	–	V
V_{OL}	LOW level output voltage	$–I_o = 2$ mA	–	–	0.4	V
Outputs SBDA, SBCL, SBWS, FDAF, FDAC, SCL, SWS, SDA, LTDATA in 3-state						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
I_I	input current	$V_i = V_{DD}$; $T_{amb} = 25$ °C	40	–	250	µA
Input/output SBMCLK						
V_{OH}	HIGH level output voltage	$+I_o = 8$ mA	$V_{DD}–0.5$	–	–	V
V_{OL}	LOW level output voltage	$–I_o = 8$ mA	–	–	0.4	V
Output SBMCLK in 3-state						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
I_I	input current	$V_i = V_{DD}$; $T_{amb} = 25$ °C	40	–	250	µA
Input/output FS256						
V_{OH}	HIGH level output voltage	$+I_o = 12$ mA	$V_{DD}–0.5$	–	–	V
V_{OL}	LOW level output voltage	$–I_o = 12$ mA	–	–	0.4	V
Output FS256 in 3-state						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
I_I	input current	$V_i = V_{DD}$; $T_{amb} = 25$ °C	40	–	250	µA

Note

1. For load impedances representative of the application.

AC CHARACTERISTICS

T_{amb} = −40 to 85 °C; V_{DD} = 3.8 to 5.5 V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
C_I	input capacitance		–	–	10	pF
X24IN and X22IN						
f	crystal frequency at X22OUT, CLK22	note 1	21	22.5792	24	MHz
f	crystal frequency at X24OUT, CLK24	note 1	23	24.576	26	MHz
gm	mutual conductance	100 kHz	1.5	–	–	mA/V
A_v	small signal gain	$A_v = gm.R_o$	3.5	–	–	V/V
C_{fb}	feedback capacitance		–	–	5	pF
C_O	output capacitance		–	–	10	pF
Outputs						
C_O	output capacitance		–	–	10	pF
Inputs URDA, RESET, LTDATA, LTCLK, LTENA, LTCNT0, LTCNT1						
t_{SU}	setup time to X24IN		15	–	–	ns
t_{HD}	hold time to X24IN		60	–	–	ns
Outputs LTDATA, MUTEDAC, DEEMDAC, ATTDAC, SYNCDAI, FDIR, FRESET						
t_d	propagation delay from X24IN		–	–	80	ns
Inputs FDAF, FDAC, SDA, SCL, SWS						
t_{SU}	setup time to FS256		15	–	–	ns
t_{HD}	hold time to FS256		25	–	–	ns
Outputs FDAF, FDAC, SDA, SCL, SWS, FSYNC						
t_d	propagation delay from FS256		–	–	50	ns
Inputs SBDA, SBCL, SBWS, URDA, SBDIR, SBEF						
t_{SU}	setup time to SBMCLK		15	–	–	ns
t_{HD}	hold time to SBMCLK		25	–	–	ns
Outputs SBDA, SBCL, SBWS						
t_d	propagation delay from SBMCLK		–	–	50	ns
FS256						
T	FS256 cycle time	f_s = 48 kHz	–	81.4	–	ns
T	FS256 cycle time	f_s = 44.1 kHz	–	88.6	–	ns
T	FS256 cycle time	f_s = 32 kHz	–	122.1	–	ns
T_C	SCL cycle time		–	4T	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FS256 master mode (FS256,SCL and SWS are output)						
t_{fH}	FS256 HIGH time	f_S = 48 kHz	35	–	–	ns
t_{fH}	FS256 HIGH time	f_S = 44.1 kHz	38	–	–	ns
t_{fH}	FS256 HIGH time	f_S = 32 kHz	75	–	–	ns
t_{fL}	FS256 LOW time	f_S = 48 kHz	35	–	–	ns
t_{fL}	FS256 LOW time	f_S = 44.1 kHz	38	–	–	ns
t_{fL}	FS256 LOW time	f_S = 32 kHz	75	–	–	ns
t_{sH}	SCL HIGH time		2T-20	–	–	ns
t_{sL}	SCL LOW time		2T-20	–	–	ns
t_S	SDA, FDAF, FDAC input setup time before FS256 HIGH		20	–	–	ns
t_{H1}	SDA, FDAF, FDAC input hold time after FS256 HIGH		30	–	–	ns
t_{H2}	SDA, FDAF, FDAC output hold time after FS256 HIGH		0	–	–	ns
$t_{D1,2}$	FS256 HIGH-to SCL, SWS, SDA, FDAF, FDAC output valid		–	–	50	ns
FS256 slave mode (FS256, SCL and SWS are input)						
t_{fH}	FS256 HIGH time		35	–	–	ns
t_{fL}	FS256 LOW time		35	–	–	ns
t_{sH}	SCL HIGH time		T+35	–	–	ns
t_{sL}	SCL LOW time		T+35	–	–	ns
t_{H1}	SDA, FDAF, FDAC output hold time after SCL HIGH		2T-15	–	–	ns
t_D	SCL HIGH-to SDA, FDAF, FDAC output valid		–	–	3T+60	ns
t_S	SDA, FDAF, FDAC input valid after SCL HIGH		20	–	–	ns
t_{H2}	SDA, FDAF, FDAC input hold time after SCL HIGH		T+20	–	–	ns
SBMCLK						
T	SBMCLK cycle time		120	163	205	ns
t_{mH}	SBMCLK HIGH time		35	–	–	ns
t_{mL}	SBMCLK LOW time		75	–	–	ns

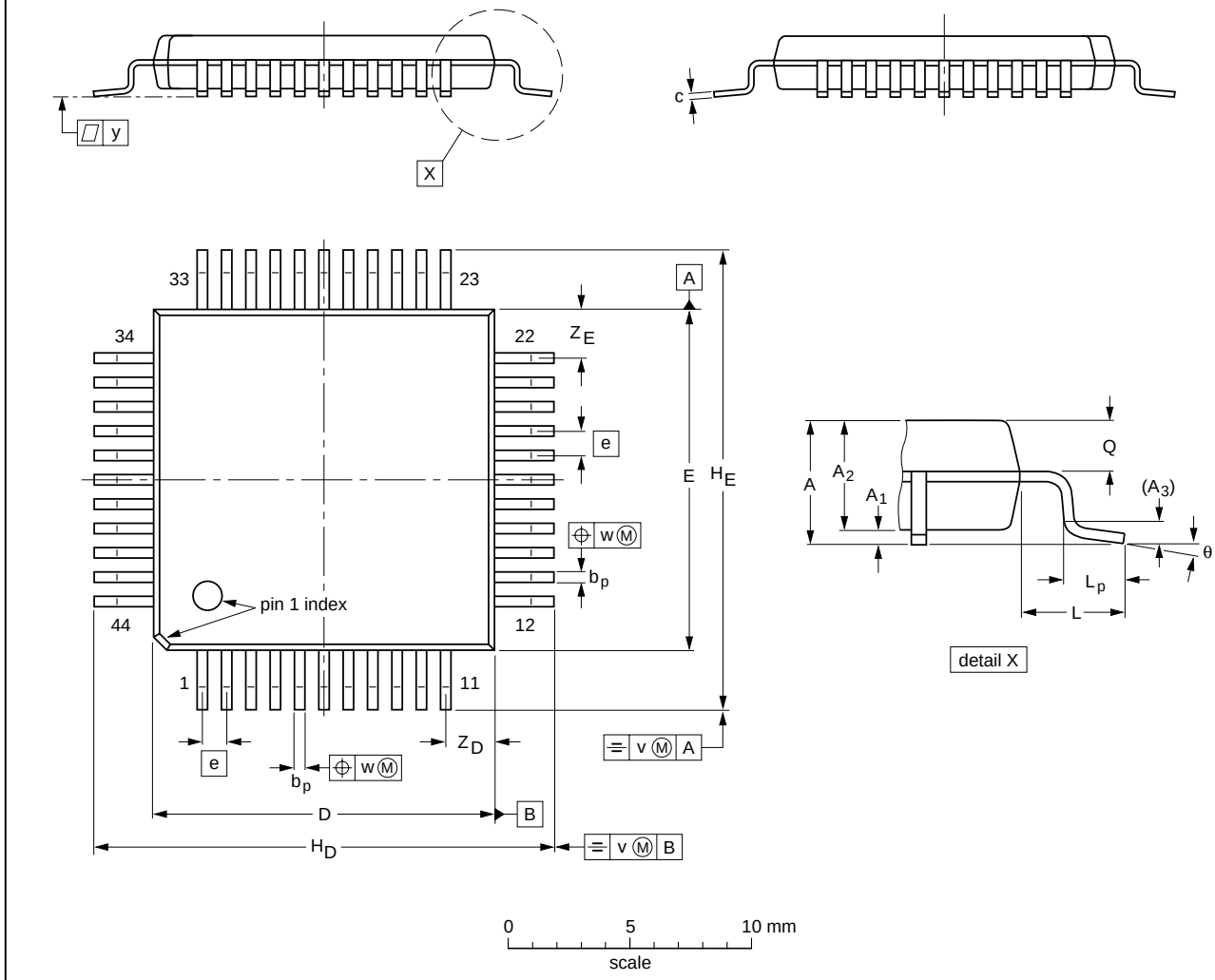
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SBMCLK master mode (SBCL, SBWS and SBDA are output)						
T_C	SBCL cycle time	384 kB/s	–	8T	–	ns
T_C	SBCL cycle time	256 kB/s	–	12T	–	ns
T_C	SBCL cycle time	192 kB/s	–	16T	–	ns
T_C	SBCL cycle time	128 kB/s	–	24T	–	ns
t_{cH}	SBCL HIGH time	384 kB/s	4T – 20	–	–	ns
t_{cH}	SBCL HIGH time	256 kB/s	6T – 20	–	–	ns
t_{cH}	SBCL HIGH time	192 kB/s	8T – 20	–	–	ns
t_{cH}	SBCL HIGH time	128 kB/s	12T – 20	–	–	ns
t_{cL}	SBCL LOW time	384 kB/s	4T – 20	–	–	ns
t_{cL}	SBCL LOW time	256 kB/s	6T – 20	–	–	ns
t_{cL}	SBCL LOW time	192 kB/s	8T – 20	–	–	ns
t_{cL}	SBCL LOW time	128 kB/s	12T – 20	–	–	ns
t_{D1}	SBWS, SBDA hold	to SBCL LOW	20	–	–	ns
t_{D2}	SBWS, SBDA valid	after SBCL 0	–	–	20	ns
SBMCLK slave mode (SBCL, SBWS and SBDA are input)						
T_C	SBCL cycle time	note 2	6.86T	8T	96T	ns
t_{cH}	SBCL HIGH time		T + 30	–	–	ns
t_{cL}	SBCL LOW time		T + 30	–	–	ns
t_{S1}	SBWS, SBDA setup time	before SBCL HIGH	T + 30	–	–	ns
t_{H1}	SBWS, SBDA hold time	after SBCL HIGH	30	–	–	ns
t_{S2}	delay before SBEF valid	after SBCL HIGH	–	–	T – 30	ns
t_{H2}	SBEF hold time	after SBCL HIGH	2T – 30	–	–	ns

Notes

1. % deviation from nominal frequency must be the same for X24, X22, and FS256 inputs to within 0.2%
2. Minimum value for bit rate = 448 kB/s
   Typical value for bit rate = 384 kB/s
   Maximum value for bit rate = 32 kB/s

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm **SOT205-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	1.2 0.9	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT205-1	133E01A					~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.